LISTING OF CLAIMS:

The following listing of claims replaces all previous versions and listings in the present application.

Please cancel claims 10-19 without prejudice or disclaimer.

1. (Currently amended) A semiconductor device comprising:

a first field effect transistor including a source and a gate and disposed in a silicon carbide substrate; and

a second field effect transistor including a drain and a gate and disposed in the substrate,

wherein the first field effect transistor is a vertical type junction field effect transistor having the source, the gate, a drain and a channel,

wherein the second field effect transistor is a lateral type junction field effect transistor having a source, the gate, the drain and a channel,

wherein the drain of the second field effect transistor connects to the source of the first field effect transistor, ~~and~~

wherein the gate of the second field effect transistor connects to the gate of the first field effect transistor, wherein the source of the vertical type junction field effect transistor is disposed on an opposite side of the drain of the vertical type junction field effect transistor, and

wherein the source of the lateral type junction field effect transistor is disposed on a same side of the drain of the lateral type junction field effect transistor.

2. (Currently amended) The device according to claim 1, further comprising:

a metal-oxide semiconductor field-effect transistor including a drain and a source and disposed in [a]the silicon carbide substrate,

wherein the second field effect transistor further includes a source,

wherein the drain of the metal-oxide semiconductor field-effect transistor connects to the source of the second field effect transistor, and

wherein the source of the metal-oxide semiconductor field-effect transistor connects to the gate of the second field effect transistor.

3. (Original) The device according to claim 2,

wherein the metal-oxide semiconductor field-effect transistor becomes an on-state in a case where the gate of the metal-oxide semiconductor field-effect transistor is applied with a gate voltage in a range between 5 volts and 10 volts.

4. (Withdrawn – currently amended) A semiconductor device comprising:

a first vertical type junction field effect transistor having a source and a gate and disposed in a silicon carbide substrate; and

a second lateral type junction field effect transistor having a drain and a source and disposed in the substrate,

wherein the drain of the second field effect transistor connects to the source of the first field effect transistor, and

wherein the source of the second field effect transistor connects to the gate of the first field effect transistor.

5. (Currently amended) ~~The device according to claim 1,~~A semiconductor device comprising:

a first field effect transistor including a source and a gate and disposed in a silicon carbide substrate; and

a second field effect transistor including a drain and a gate and disposed in the substrate,

wherein the drain of the second field effect transistor connects to the source of the first field effect transistor,

wherein the gate of the second field effect transistor connects to the gate of the first field effect transistor,

wherein the substrate includes:

a first layer made of silicon carbide and heavily doped with a first impurity having a first type conductivity;

a second layer made of silicon carbide and lightly doped with the first impurity; and

a third layer made of silicon carbide and moderately doped with the first impurity,

wherein the second layer is disposed on the first layer, and the third layer is disposed on the second layer,

wherein the substrate further includes:

a first impurity diffusion region heavily doped with the first impurity; and

a second impurity diffusion region heavily doped with a second impurity having a second type conductivity,

wherein the second impurity diffusion region is disposed in the second layer near a boundary between the second layer and the third layer, and covers a predetermined area of the boundary,

wherein the third layer has first, second and third surface portions, and the first impurity diffusion region is disposed in each of the first, second and third surface portions of the third layer,

wherein the first field effect transistor is a vertical type junction field effect transistor having the source, the gate, a drain and a channel,

wherein the source of the first field effect transistor is the first impurity diffusion region disposed in the first surface portion, the drain of the first field effect transistor is the first layer, the gate of the first field effect transistor is the second impurity diffusion region, and the channel of the first field effect transistor is a part of the second layer near the boundary between the second layer and the third layer, the part of the second layer not being covered with the second type impurity diffusion region,

wherein the second field effect transistor is a lateral type junction field effect transistor having a source, the gate, the drain and a channel,

wherein the source of the second field effect transistor is the first impurity diffusion region disposed in the second surface portion, the drain of the second field effect transistor is the first impurity diffusion region disposed in the third surface portion, the gate of the second field effect transistor is the second impurity diffusion region, and the channel of the second field effect transistor is the third layer, and

wherein the second surface portion separates from the third surface portion.

6. (Withdrawn) The device according to claim 4,

wherein the substrate includes:

a first layer made of silicon carbide and heavily doped with a first impurity having a first type conductivity;

a second layer made of silicon carbide and lightly doped with the first impurity; and

a third layer made of silicon carbide and moderately doped with the first impurity,

wherein the second layer is disposed on the first layer, and the third layer is disposed on the second layer,

wherein the substrate further includes:

a first impurity diffusion region heavily doped with the first impurity; and

a second impurity diffusion region heavily doped with a second impurity having a second type conductivity,

wherein the second impurity diffusion region is disposed in the second layer near a boundary between the second layer and the third layer, and covers a predetermined area of the boundary,

wherein the third layer has first, second and third surface portions, and the first impurity diffusion region is disposed in each of the first, second and third surface portions of the third layer,

wherein the first field effect transistor is a vertical type junction field effect transistor having the source, the gate, a drain and a channel,

wherein the source of the first field effect transistor is the first impurity diffusion region disposed in the first surface portion, the drain of the first field effect transistor is the first layer, the gate of the first field effect transistor is the second impurity diffusion region, and the channel of the first field effect transistor is a part of the second layer near the boundary between the second layer and the third layer, the part of the second layer not being covered with the second type impurity diffusion region,

wherein the second field effect transistor is a lateral type accumulation mode field effect transistor having the source, a gate, the drain and a channel,

wherein the source of the second field effect transistor is the first impurity diffusion region disposed in the second surface portion, the drain of the second field effect transistor is the first impurity diffusion region disposed in the third surface portion, the gate of the second field effect transistor is provided by an electrode disposed on the third layer through an insulation film and disposed between the second and third surface portions, and the channel of the second field effect transistor is the third layer, and

wherein the second surface portion separates from the third surface portion.

7. (Withdrawn) The device according to claim 4,

wherein the substrate includes:

a first layer made of silicon carbide and heavily doped with a first impurity having a first type conductivity;

a second layer made of silicon carbide and lightly doped with the first impurity; and

a third layer made of silicon carbide and moderately doped with the first impurity,

wherein the second layer is disposed on the first layer, and the third layer is disposed on the second layer,

wherein the substrate further includes:

a first impurity diffusion region heavily doped with the first impurity having the first type conductivity;

a second impurity diffusion region heavily doped with a second impurity having a second type conductivity; and

a third impurity diffusion region moderately doped with the second impurity,

wherein the second impurity diffusion region is disposed in the second layer near a boundary between the second layer and the third layer, and covers a predetermined area of the boundary,

wherein the third layer has first, second and third surface portions, and the third impurity diffusion region is disposed in a fourth surface portion of the third layer,

wherein the first impurity diffusion region is disposed in each of the first, second and third surface portions of the third layer,

wherein the first field effect transistor is a vertical type junction field effect transistor having the source, the gate, a drain and a channel,

wherein the source of the first field effect transistor is the first impurity diffusion region disposed in the first surface portion, the drain of the first field effect transistor is the first layer, the gate of the first field effect transistor is the second impurity diffusion region, and the channel of the first field effect transistor is a part of the second layer near the boundary between the second layer and the third layer, the part of the second layer without covering with the second impurity diffusion region,

wherein the second field effect transistor is a lateral type inverse mode field effect transistor having the source, a gate, the drain and a channel,

wherein the source of the second field effect transistor is the first impurity diffusion region disposed in the second surface portion, the drain of the second field effect transistor is the first impurity diffusion region disposed in the third surface portion, the gate of the second field effect transistor is provided by an electrode disposed on the third impurity diffusion region through an insulation film and disposed between the second and third surface portions, and the channel of the second field effect transistor is the third impurity diffusion region, and

wherein the second surface portion separates from the third surface portion, and the second and third surface portions contact the third impurity diffusion region.

8. (Original) The device according to claim 5, further comprising:

a separation disposed in the third layer and reaches the second impurity diffusion region,

wherein the separation separates the third layer into a first part and a second part, and

wherein the source of the first field effect transistor is disposed in the first part, and the second field effect transistor is disposed in the second part.

9. (Original) The device according to claim 8,

wherein the second impurity diffusion region covers almost whole area of the boundary between the second layer and the third layer except for the channel of the first field effect transistor, and

wherein the second impurity diffusion region separates between the second part and the second layer.

10. – 19. (Canceled)